substantially wider than a portion of the stable inner lead that does not contact the adhesive member.

B1 Concl'd

5. The LOC type semiconductor package as claimed in claim 2, wherein the ends of the general inner leads are up-set toward the top of the semiconductor chip.

REMARKS

Claims 1-5 were pending at the time of examination. Claims 1-3 stand rejected under 35 USC §103(a) as being unpatentable over Russell; and claims 4 and 5 stand rejected under 35 USC §103(a) as being unpatentable over Lee in view of Takeuchi and Tsubosaki et al. Applicant has amended claim 1. In view of the amendments and arguments set forth herein, Applicant respectfully submits that claims 1-5 are in condition for allowance.

I. 35 USC §103(a) Rejection of Claims 1-3.

At page 2 of the Office Action, the Examiner rejected claims 1-3 under 35 USC §103(a) as being obvious over Russell. Applicant respectfully traverses this rejection.

According to MPEP §706.02(j), "[t]o establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine the reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found

LAW OFFICES OF
SKJERVEN MORRILL LLP
3 EMBARCADERO CENTER
SUITE 2800
SAN FRANCISCO, CA 94111
(415) 217-6000
FAX (415) 434-0646

in the prior art and not based on Applicants' disclosure." Applicant respectfully notes that in the present case, Russell does not teach or suggest all of the elements of amended claim 1, and therefore cannot make claims 1-3 obvious.

Applicant has amended claim 1 to recite that there are "at most *four* stable leads". This provides an advantage over prior art types of LOC packages, such as that disclosed in Russell, where "the shapes of the leads depend on the size of the semiconductor chip." See Applicant's specification, page 6, lines 6-7. In particular, in contrast to the arrangement of Russell where almost *all* leads are acting as "stable" leads, the Applicant's claimed arrangement with "at most four stable leads" allows flexibility for use with a wide variety of different size chips. Because almost all of the leads in Russell are acting as "stabilizing" leads, and because there are much more than four of such leads, Russell does not teach or suggest "at most four stable leads" as recited in Applicant's claim 1.

Accordingly, Applicant respectfully submits that amended claim 1 has not been made obvious by Russell, and that the Examiner's §103(a) rejection of claim 1 cannot stand. Therefore, an allowance of claim 1 is respectfully requested. Furthermore, an allowance of claims 2 and 3, which are dependent on claim 1, is respectfully requested as well for at least the same reasons.

II. 35 USC §103(a) Rejection of Claims 4 and 5.

At page 4 of the Office Action, the Examiner rejected claims 4 and 5 under 35 USC §103(a) as being obvious over Russell in view of Takeuchi and Tsubosaki at al. Applicants respectfully traverse this rejection.

Claims 4 and 5 depend from claim 1 which, as discussed above, should be in condition for allowance. Therefore, Applicant believes the Examiner's §103(a) rejection of claims 4

LAW OFFICES OF
SKJERVEN MORRILL LLP

3 EMBARCADERO CENTER
SUITE 2800
SAN FRANCISCO, CA 94111
(415) 217-6000
FAX (415) 434-0646

and 5 has been made moot in view of the amendments to claim 1, and allowance of these claims is respectfully requested.

III. Conclusion

Applicant respectfully submits that in view of the above claim amendments and remarks, the Examiner's rejections of claims 1-5 have been overcome. Thus, it is believed that all claims are in condition for allowance, and a notice of allowance is respectfully requested. Should the Examiner have any questions, or otherwise wish to discuss this case, please contact the undersigned at (415) 217-6000.

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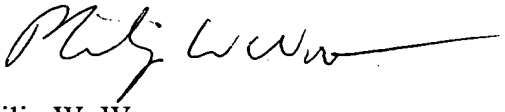
Respectfully submitted,



Philip W. Woo
Attorney of Record
Reg. No. 39,880

LAW OFFICES OF
SKJERVEN MORRILL LLP

3 EMBARCADERO CENTER
SUITE 2800
SAN FRANCISCO, CA 94111
(415) 217-6000
FAX (415) 434-0646

Version with markings to show changes made

For the convenience of the Examiner, all pending claims are provided below, whether amended or not. Unamended claims are shown in italics for the convenience of the Examiner.

1. (Amended.) An LOC type semiconductor package, comprising:

a semiconductor chip on which a plurality of bonding pads are arranged in a row;

leads that correspond to the bonding pads, the leads being located on opposite sides of the semiconductor chip with the bonding pads therebetween;

wires electrically connecting the bonding pads to the leads; and

a molding resin encapsulating the semiconductor chip, leads and wires, wherein:

the leads include a plurality of general leads and [a pair of] at most four stable leads;

the at most four stable leads are electrically connected to the bonding pads via the wires, [disposed at opposite ends of the semiconductor chip, and bent to] extend toward the semiconductor chip, and are physically [contact] affixed to the semiconductor chip [to fix the semiconductor chip]; and

the general leads are [disposed in a row between alongside the stable leads,] electrically connected to the bonding pads by way of the wires, and separated from the semiconductor chip, thereby coming into no physical contact with the semiconductor chip.

2. The LOC type semiconductor package as claimed in claim 1, wherein:

the general leads include general inner leads encapsulated in the molding resin and general outer leads extending from the molding; and

the stable leads include stable inner leads encapsulated in the molding resin and stable outer leads extending from the molding resin.

LAW OFFICES OF
SKJERVEN MORRILL LLP

3 EMBARCADERO CENTER
SUITE 2800
SAN FRANCISCO, CA 94111
(415) 217-6000
FAX (415) 434-0646

3. The LOC type semiconductor package as claimed in claim 2, wherein an adhesive member is on the portion of the surface of the semiconductor chip, corresponding to the end of each of the stable inner leads, to fix the end of the stable inner lead onto the surface of the semiconductor chip.

4. The LOC type semiconductor package as claimed in claim 3, wherein the surface area of the end of the stable inner lead coming into contact with the adhesive member is substantially wider than a portion of the stable inner lead that does not contact the adhesive member.

5. The LOC type semiconductor package as claimed in claim 2, wherein the ends of the general inner leads are up-set toward the top of the semiconductor chip.

LAW OFFICES OF
SKJERVEN MORRILL LLP

3 EMBARCADERO CENTER
SUITE 2800
SAN FRANCISCO, CA 94111
(415) 217-6000
FAX (415) 434-0646